

**Amendments to the Claims:**

Claims 1, 11 and 18 are currently amended. Claims 2 – 3, 6 – 10, 12, 14 – 17 and 19 – 20 are previously presented. Claims 4 – 5 and 13 are original. No new matter is added by these amendments. Consideration of all amendments is respectfully requested.

5 **Listing of Claims:**

Claim 1 (currently amended): A method for determining whether a memory is the  
integrity of a possibly-defected or has integrity memory under a plurality of  
operating environments comprising:  
10           setting a plurality of operating environments respectively corresponding to  
              variations in a condition to be tested;  
              repeatedly testing the same memory under each of the plurality of operating  
              environments;  
              recording a result of the testing step for each of the plurality of operating  
              environments; and  
15           comparing the recorded results for each of the plurality of operating  
              environments, wherein if the results are the same for each of the plurality  
              of operating environments then the memory is determined to have  
              integrity.

20    Claim 2 (previously presented): The method of claim 1, wherein the testing step further  
          comprises:  
          performing a built-in self test (BIST) on the memory under each of the plurality  
          of operating environments.

25    Claim 3 (previously presented): The method of claim 2 further comprising:  
          marking a status record memory according to the BIST, wherein the status record  
          memory corresponds to the memory; and

recording the content of the status record memory for each of the plurality of  
operating environments.

5        Claim 4 (original): The method in claim 1 wherein the condition to be tested is a variance  
in supply voltage.

Claim 5 (original): The method in claim 1 wherein the condition to be tested is a variance  
in temperature.

10      Claim 6 (previously presented): The method of claim 1 wherein the testing step further  
comprises:  
detecting information concerning defects in the memory; and  
counting the number of defects in the memory under each of the plurality of  
operating environments.

15      Claim 7 (previously presented): The method in claim 6 wherein the recording step further  
comprises:  
storing the number of defects detected in the memory.

20      Claim 8 (previously presented): The method in claim 7 wherein the comparing step  
further comprises:  
accessing the stored number of defects to determine if the numbers of defects  
detected in the memory under each of the plurality of operating  
environments are equal to one another;  
25      wherein if the numbers of defects detected in the memory under each of the  
plurality of operating environments are equal to one another then the  
memory is determined to have integrity.

Claim 9 (previously presented): The method in claim 6 wherein the recording step further comprises:  
recording and storing the position of each defect detected in the memory under each of the plurality of operating environments.

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Claim 10 (previously presented): The method in claim 9 wherein the comparing step further comprises:  
determining if the positions of defects of the memory under each of the plurality of operating are the same as one another.

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Claim 11 (currently amended): A method for determining ~~whether a memory is the integrity of a possibly-defected~~ or has integrity-memory, comprising:  
testing the memory under a first operating environment corresponding to a condition to be tested;  
15 recording a first result of the testing step under the first operating environment;  
testing the memory under a second operating environment, wherein the second operating environment corresponds to a variation of the condition to be tested in the first operating environment;  
recording a second result of the testing step under the second operating  
20 environment; and  
comparing the first result with the second result, wherein if the first result is equal to the second result then the memory is determined to have integrity.

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Claim 12 (previously presented): The method of claim 11 wherein the testing steps further comprise:  
performing a built-in self test (BIST) on the memory.

Claim 13 (original): The method of claim 12 further comprising:

marking a status record memory according to the BIST, wherein the status  
record memory corresponds to the memory; and  
recording the content of the status record memory for the current operating  
environment.

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Claim 14 (previously presented): The method in claim 11 wherein the condition to be  
tested in the first and the second operating environment is supply voltage.

10 Claim 15 (previously presented): The method in claim 11 wherein the condition to be  
tested in the first and the second operating environment is temperature.

Claim 16 (previously presented): The method in claim 11 further comprising:  
determining whether the first and second results are consistent or inconsistent  
with one another.

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Claim 17 (previously presented): The method in claim 11 wherein the first result  
comprises information of defect locations in the memory corresponding to the  
first operating environment and the second result comprises information of  
defect locations in the memory corresponding to the second operating  
20 environment.

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Claim 18 (currently amended): A method for determining integrity of a memory with  
sections that are ~~possibly~~ defective, the method comprising:  
repeatedly testing the memory under a plurality of operating environments  
25 respectively corresponding to a given condition to be tested;  
recording a result of the testing step for each of the plurality of operating  
environments;  
comparing the results; and

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determining whether the results are consistent or inconsistent with one another;  
wherein the results correspond to the given condition, and if they are consistent  
with one another the memory is determined to have integrity.

- 5     Claim 19 (previously presented): The method in claim 18 wherein the first result  
comprises information regarding the number of defective sections in the  
memory corresponding to the first operating environment and the second result  
comprises information regarding the number of defective sections in the  
memory corresponding to the second operating environment.

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- Claim 20 (previously presented): The method in claim 18 wherein the first result  
comprises information regarding locations of defective sections in the memory  
corresponding to the first operating environment and the second result  
comprises information regarding locations of defective sections in the memory  
15     corresponding to the second operating environment.